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EXAMINER INTERVIEW AGENDA

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Dear Examiner Kim:

Please find attached hereto an Examiner Interview Agenda (regarding Application No. 10/045,297 – COMMUNICATIONS ARCHITECTURE FOR MEMORY-BASED DEVICES, filed November 7, 2001) for your consideration.

Thank you for granting a personal interview with myself and Dr. Dongyun Lee, Sr. Design Manager for Silicon Image on January 23, 2007 at 11:00 am. We thank you in advance for your time and effort in this regard.

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Docket No.: 594728812US
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Lee et al.

Application No.: 10/045,297

Confirmation No.: 1257

Filed: November 7, 2001

Art Unit: 2185

For: COMMUNICATIONS ARCHITECTURE FOR
MEMORY-BASED DEVICES

Examiner: H.C. KIM

EXAMINER INTERVIEW AGENDA

Examiner Kim,

In reference to the Non-Final Office Action, dated November 21, 2006, and to the granted request for an in-person interview to be held at the United States Patent Office at 11:00 a.m. on Tuesday, January 23, 2007, applicants respectfully submit the following agenda for your consideration:

AGENDA FOR INTERVIEW

1. A discussion of the proposed amendments to the claims that are provided in Attachment A to this agenda. Points to be discussed:

- A. Summary of applicants' technology and claim amendments.
- B. Discussion of claimed features not found in the prior art.

For example, applicants respectfully submit that Sonnier et al., Davidson et al., and Knecht et al. fail to disclose a memory device having a plurality of serial communication ports connected to a plurality of memory banks by a switch. Such construction is depicted in Figure 30 and at other locations in applicants' drawings and specification.

In addition, applicants respectfully submit that Sonnier et al., Davidson et

al., and Knecht et al. fail to disclose a memory device.

2. A discussion of the restriction requirement of claim 37-40.
3. A discussion of any new prior art. Points to be discussed:
 - A. An introduction of any new prior art.
 - B. Discussion of elements that distinguish applicants' technology from new prior art references.
4. Any other considerations.

CONCLUSION

Applicants thank the Examiner in advance for the interview with the undersigned and with Dr. Dongyun Lee, Sr. Design Manager for Silicon Image. Should additional information be required, the Examiner is encouraged to contact the undersigned representative.

Dated: January 18, 2006

Respectfully submitted,

By 
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Attachment A

1. (Currently Amended) A memory device couplable to a plurality of accessing devices, the memory device comprising:

a memory comprising a plurality of banks; and

a plurality of ports for accessing the plurality of banks ~~memory~~ of the memory device, each port having a bit serial communications link for receiving from and transmitting to an accessing device where bits of each symbol are received and transmitted serially, each port using a plesiosynchronous technique without transmitting a clock signal to receive symbols and using in-band symbols to transmit data and out-of-band symbols to transmit control information; and

a switch for selectively connecting the plurality of ports to the plurality of banks.

2. (Previously Presented) The memory device of claim 1 wherein each bit serial communications link is connected to an accessing device via a point-to-point connection.

3. (Previously Presented) The memory device of claim 1 wherein the plesiosynchronous technique oversamples data received via the bit serial communications link.

4. (Previously Presented) A memory device comprising:

a memory; and

a plurality of ports for accessing the memory of the memory device, each port having a serial communications link for receiving from and transmitting to an accessing device, each port using plesiosynchronous technique to receive symbols and using in-band symbols to transmit data and out-of-band symbols to transmit control information wherein each port includes a

line driver with a fixed driver portion and a variable driver portion for DC-balancing.

5. (Currently Amended) The memory device of claim 1 wherein the ~~memory includes multiple banks and wherein multiple~~ plurality of banks can be simultaneously accessed by different ports.

6. (Currently Amended) The memory device of claim ~~5~~ 1 wherein each bank includes multiple sections and wherein the multiple sections can be simultaneously accessed by different ports.

7. (Cancelled) ~~The memory device of claim 1 wherein the memory includes a bank with multiple sections and wherein the multiple sections can be simultaneously accessed by different ports.~~

8. (Currently Amended) The memory device of claim ~~7~~ 6 wherein the multiple sections of the bank are configurable on a port-by-port basis.

9. (Original) The memory device of claim 8 wherein the configuration information indicates to enable certain sections of the bank.

10. (Original) The memory device of claim 1 wherein the ports are connected to the memory using time-division multiplexing.

11. (Cancelled) ~~The memory device of claim 1 wherein the ports are connected to the memory using a crossbar switch.~~

12. (Original) The memory device of claim 1 wherein control information is transmitted as a primitive.

13. (Original) The memory device of claim 12 wherein a primitive includes two out-of-band symbols.

14. (Original) The memory device of claim 12 wherein control information includes a synchronization symbol.

15. (Original) The memory device of claim 1 wherein the plesiosynchronous technique includes inserting or removing symbols to compensate for variations between clock frequencies of the accessing device and the memory device.

16. (Original) The memory device of claim 1 wherein the ports share a single multiphase clock generator.

17. (Original) The memory device of claim 16 wherein the multiphase clock generator is a phase lock loop.

18. (Original) The memory device of claim 1 wherein an out-of-band symbol is a synchronization symbol that encodes a memory command.

19. (Currently Amended) A memory device comprising: a memory comprising a plurality of banks that reads and writes data; a multiphase clock generator that provides a multiphase clock signal; and a plurality of ports for accessing the plurality of banks, each port for connecting to a bit serial communications link, where bits of each symbol are received and transmitted serially, and for receiving data and control information via the bit serial communications link using a plesiosynchronous technique without transmitting a clock signal, wherein each port uses the generated multiphase clock signal generated by the multiphase clock generator; and a switch for selectively connecting the plurality of ports to the plurality of banks.

20. (Original) The memory device of claim 19 wherein data is sent using in-band symbols and control information is sent via out-of-band symbols.

21. (Previously Presented) The memory device of claim 19 wherein each bit serial communications link is connected to an accessing device via a point-to-point connection.

22. (Previously Presented) The memory device of claim 19 wherein the plesiosynchronous technique oversamples data received via the bit serial communications link.

23. (Previously Presented) A memory device comprising: a memory that reads and writes data; a multiphase clock generator that provides a multiphase clock signal; and a plurality of ports, each port for connecting to a serial communications link and for receiving data and control information via the serial communications link using a plesiosynchronous technique, wherein each port uses the generated multiphase clock signal generated by the multiphase clock generator and wherein each port includes a line driver with a fixed driver portion and a variable driver portion for DC-balancing.

24. (Currently Amended) The memory device of claim 19 wherein the ~~memory includes multiple banks and wherein multiple~~ plurality of banks can be simultaneously accessed by different ports.

25. (Currently Amended) The memory device of claim ~~24~~ 19 wherein each bank includes multiple sections and wherein multiple sections can be simultaneously accessed by different ports.

26. (Cancelled) ~~The memory device of claim 19 including multiple sections and wherein multiple sections can be simultaneously accessed by different ports.~~

27. (Original) The memory device of claim 26 wherein the multiple sections are configurable on a port-by-port basis.

28. (Original) The memory device of claim 27 including the configuration information storage.

29. (Original) The memory device of claim 19 wherein the ports are connected to the memory using time-division multiplexing.

30. ~~(Cancelled) The memory device of claim 19 wherein the ports are connected to the memory using a crossbar switch.~~

31. (Original) The memory device of claim 19 wherein control information is transmitted as a primitive.

32. (Original) The memory device of claim 31 wherein a primitive includes two out-of-band symbols.

33. (Original) The memory device of claim 31 wherein control information includes a synchronization symbol.

34. (Original) The memory device of claim 19 wherein the plesiosynchronous technique includes inserting or removing symbols to compensate for variations between clock frequencies of the accessing device and the memory device.

35. (Original) The memory device of claim 19 wherein the multiphase clock generator is a phase lock loop.

36. (Original) The memory device of claim 19 wherein a synchronization symbol encodes a memory command.

37. (Previously Presented) A propagated serial data signal conveying information between an accessing device and a memory device, the propagated serial data signal comprising:

an in-band symbol component for conveying data; and
an out-of-band symbol component for conveying control information, wherein the control information excludes a clock signal but includes a synchronization symbol to allow for the compensation of variations between clock frequencies of the accessing device and the memory device.

38. (Previously Presented) The propagated serial data signal of claim 37 wherein the control information is conveyed as a primitive.

39. (Previously Presented) The propagated serial data signal of claim 38 wherein the primitive comprises two symbols.

40. (Previously Presented) The propagated serial data signal of claim 37 wherein the synchronization symbol encodes a memory command.